REMARKS

In the final rejection, the original rejection was supplemented with citations apparently from the brief summary of the invention. This is problematic because the previous rejection relied on the material in the background of the invention. Now what we have is two different embodiments combined, which really does not make any sense.

The brief summary of the invention summarizes what is set forth in greater detail in paragraphs 39-45. In the event of a miss, the TLB control 70 provides a signal that there is no match in the TLB memory 72. See paragraph 39. There are two approaches to this problem. In the first approach, a hardware approach, described in paragraph 41, "the virtual address, resource identifier and task identifier presented to a logical circuit." See paragraph 41.
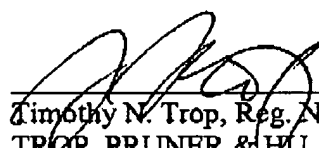
There is no conversion logic to generate a <u>modified</u> virtual address from the virtual address if a virtual address to physical address translation for the virtual address does not exist in the storage. Instead, the virtual address itself is utilized, not a modified virtual address. Moreover, the claim requires a page table walk unit configured to convert the modified virtual address into the corresponding physical address. This, too, cannot exist in the cited reference because there never is a modified virtual address.

The software embodiment, described in paragraph 45 is said to operate similarly.

Thus, neither embodiment in any way supplements the deficiencies of the embodiment of the background of the invention described in paragraphs 7 and 8. Therefore, a *prima facie* rejection is not made out and reconsideration would be appropriate.

Respectfully submitted,

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Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
1616 South Voss Road, Suite 750
Houston, TX 77057-2631
713/468-8880 [Phone]
713/468-8883 [Fax]

Attorneys for Intel Corporation

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